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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete, if known	
				Application Number	10/720,562
				Filing Date	11/24/2003
				First Named Inventor	Correale, Jr. et al.
				Art Unit	2925
				Examiner Name	GARBOWSKI
				Attorney Docket Number	YOR920030359US1
Sheet	1	of	2		

[illegible][illegible]

Examiner Signature		Date Considered	10/18/5
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449B/PTO		Complete if Known			
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10/720,562		
		Filing Date	11/24/2003		
		First Named Inventor	Correale, Jr. et al.		
		Art Unit	2825		
		Examiner Name	GARBOWSKI		
Sheet	2	of	2	Attorney Docket Number	YOR920030359US1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials ^a	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
W		LACKEY ET AL., Managing power and performance for System-on-Chip designs using Voltage Islands, Proceedings of the 2002 IEEE/ACM International conference on Computer-aided design, 11/11/2002, Page(s) 195-202	
W		USAMI ET AL., CLUSTERED VOLTAGE SCALING TECHNIQUES FOR LOW-POWER DESIGN, International Symposium on Low-Power Electronic Design, 4/1/1995, Page(s) 3-8, Publisher: ACM Press	
W		USAMI ET AL., AUTOMATED LOW-POWER TECHNIQUE EXPLOITING MULTIPLE SUPPLY VOLTAGES APPLIED TO A MEDIA PROCESSOR, IEEE Journal of Solid-State Circuits, 3/1/1998, Page(s) 463-472, Volume 33, Number 3	
W		YEH ET AL., LAYOUT TECHNIQUES SUPPORTING THE USE OF DUAL SUPPLY VOLTAGES FOR CELL-BASED DESIGNS, Proc. ACM/IEEE Design Auto. Conf., 6/1/1999, Page(s) 62-67	

Examiner Signature		Date Considered	10/18/05
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